## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application.

**Listing of Claims:**

1. (Currently amended) A pixel cell comprising:

a first ~~photo-conversion device~~ pinned photodiode that generates charge;

a second ~~photo-conversion device~~ pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

readout circuitry that provides first readout signals indicating charge generated by the first ~~device~~ pinned photodiode and second readout signals indicating charge generated by the second ~~device~~ pinned photodiode.

2-3. (Canceled).

4. (Currently amended) The pixel cell of claim 1, wherein the second ~~photo-conversion device~~ pinned photodiode is a floating diffusion region.

5. (Canceled).

6. (Currently amended) The pixel cell of claim [[5]]1, ~~wherein the first photo-conversion device is a pinned photodiode, and~~ wherein the second ~~photo-conversion device~~ pinned photodiode has a higher pinning voltage than the first ~~photo-conversion device~~ pinned photodiode.

7. (Canceled).

8. (Currently amended) The pixel cell of claim 1, further comprising a second transistor having a gate ~~adjacent~~ coupled to the first ~~photo-conversion device~~ pinned photodiode, wherein the ~~first~~ second transistor is ~~one of~~ a shutter transistor for determining an integration time ~~or a transfer transistor for transferring photo-generated charge to the second photo-conversion device~~.

9. (Currently amended) The pixel cell of claim [[8]]1, wherein the first transistor is coupled to the first and second ~~photo-conversion device~~ pinned photodiodes is ~~adjacent to the transistor gate and on a side of the transistor gate opposite to the first photo-conversion device~~.

10. (Original) The pixel cell of claim 8, further comprising a doped well in the substrate below the transistor gate.

11. (Currently amended) The pixel cell of claim 1, further comprising at least one doped well in [[the]]a substrate, wherein the first and second pinned photodiodes are within the substrate.

12. (Currently amended) The pixel cell of claim 11, wherein the second ~~photo-conversion device~~ pinned photodiode is in the doped well.

13. (Currently amended) The pixel cell of claim 11, wherein the first ~~photo-conversion device~~ pinned photodiode is not in the doped well.

14. (Currently amended) The pixel cell of claim 11, wherein the ~~photo-conversion device~~ pinned photodiode is not in the doped well.

15. (Currently amended) The pixel cell of claim 14, wherein there is a doped well between the first and second ~~photo-conversion devices~~ pinned photodiodes.

16. (Currently amended) The pixel cell of claim 1, further comprising a gate of a second transistor electrically connected to the second ~~photo-conversion device~~ pinned photodiode, wherein the second transistor is an output source follower transistor.

17-23. (Canceled).

24. (Currently amended) A pixel cell comprising:

a first pinned photodiode that generates charge in response to light;

~~a first gate of a first transistor adjacent to the first pinned photodiode;~~

a second pinned photodiode that generates charge in response to light and ~~receiving~~ receives charge transferred from the first pinned photodiode;

a first transistor coupled to the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

a ~~second~~ gate of a second transistor ~~electrically connected~~coupled to the second pinned photodiode.

25. (Currently amended) An image sensor comprising:

an array of pixel cells, wherein at least two pixel cells each comprise:

a first ~~photo-conversion device~~ pinned photodiode that generates charge;

a second ~~photo-conversion device~~ pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

readout circuitry that provides first readout signals indicating charge generated by the first ~~device~~ pinned photodiode and second readout signals indicating charge generated by the second ~~device~~ pinned photodiode.

26-28. (Canceled).

29. (Currently amended) The image sensor of claim 25, wherein the second ~~photo-conversion device~~ pinned photodiode is a floating diffusion region.

30. (Canceled).

31. (Currently amended) The image sensor of claim 30, ~~wherein the first photo-conversion device is a pinned photodiode, and~~ wherein the second ~~photo-conversion device~~ pinned photodiode has a higher pinning voltage than the first ~~photo-conversion device~~ pinned photodiode.

32. (Currently amended) The image sensor of claim 25, further comprising a gate of a second transistor ~~adjacent~~ coupled to the first ~~photo-conversion device~~ pinned photodiode, wherein the second transistor is ~~one of~~ a shutter transistor

for determining an integration time ~~or a transfer transistor for transferring photo-generated charge to the second photo-conversion device~~.

33. (Currently amended) The image sensor of claim [[32]]25, wherein the first transistor is coupled to the first and second ~~photo-conversion device~~ pinned photodiodes ~~is adjacent to the transistor gate and on a side of the transistor gate opposite to the first photo-conversion device~~.

34. (Currently amended) The image sensor of claim 32, further comprising a doped well in the substrate below the transistor gate.

35. (Currently amended) The image sensor of claim 25, further comprising at least one doped well in [[the]]a substrate, wherein the first and second pinned photodiodes are within the substrate.

36. (Currently amended) The image sensor of claim 35, wherein the second ~~photo-conversion device~~ pinned photodiode is in the doped well.

37. (Currently amended) The image sensor of claim 35, wherein the first ~~photo-conversion device~~ pinned photodiode is not in the doped well.

38. (Currently amended) The image sensor of claim 35, wherein the second ~~photo-conversion device~~ pinned photodiode is not in the doped well.

39. (Currently amended) The image sensor of claim 38, wherein there is a doped well between the first and second ~~photo-conversion devices~~ pinned photodiodes.

40. (Currently amended) The image sensor of claim 25, wherein the at least two pixel cells further comprise a gate of a second transistor electrically connected to

the second ~~photo-conversion device~~ pinned photodiode, wherein the second transistor is an output source follower transistor.

41. (Currently amended) The image sensor of claim 25, further comprising control circuitry that applies a criterion to readout signals from the second ~~photo-conversion devices~~ pinned photodiodes until the criterion is met, and when the criterion is met, causes the readout circuitry to provide signals indicating charge generated by the first ~~photo-conversion devices~~ pinned photodiode.

42. (Original) The image sensor of claim 25, further comprising correlated double sampling (CDS) circuitry that performs CDS operations.

43. (Canceled).

44. (Currently amended) A processor system, comprising:

a processor;

an image sensor coupled to the processor, the image sensor comprising an array of pixel cells, wherein at least two of the pixel cells each comprise:

a first ~~photo-conversion device~~ pinned photodiode that generates charge;

a second ~~photo-conversion device~~ pinned photodiode that generates charge;

a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode;

readout circuitry that provides first readout signals indicating charge generated by the first ~~device~~ pinned photodiode and second readout signals indicating charge generated by the second ~~device~~ pinned photodiode; and

control circuitry that applies a criterion to readout signals from the second photo-conversion devices until the criterion is met, and when the criterion is met, causes the readout circuitry to provide signals indicating charge generated by the first photo-conversion devices.

45. (Original) The processor system of claim 44, wherein the image sensor further comprises correlated double sampling (CDS) circuitry that performs CDS operations.

46-47. (Canceled).

48. (Currently amended) A method of forming a pixel cell, the method comprising:

forming a first ~~photo-conversion device~~ pinned photodiode that generates charge;

forming a second ~~photo-conversion device~~ pinned photodiode that generates charge;

forming a first transistor between the first and second pinned photodiodes for transferring charge generated by the first pinned photodiode to the second pinned photodiode; and

forming readout circuitry that provides first readout signals indicating charge generated by the first ~~device~~ pinned photodiode and second readout signals indicating charge generated by the second ~~device~~ pinned photodiode.

49-51. (Canceled).

52. (Currently amended) The method of claim 48, wherein the act of forming the second ~~photo-conversion device~~ pinned photodiode comprises forming a floating diffusion region.

53. (Canceled).

54. (Currently amended) The method of claim 53, ~~wherein the act of forming the first photo-conversion device comprises forming a pinned photodiode, and~~ further comprising setting a pinning voltage for the second photo-conversion device higher than a pinning voltage for the first photo-conversion device.

55. (Currently amended) The method of claim 48, further comprising forming ~~a gate of~~ a second transistor ~~adjacent~~ coupled to the first ~~photo-conversion device~~ pinned photodiode, wherein the act of forming the second transistor ~~gate~~ comprises forming ~~the gate of one of~~ a shutter transistor for determining an integration time ~~or a transfer transistor for transferring photo-generated charge to the second photo-conversion device~~.

56. (Canceled).

57. (Currently amended) The method of claim 55, further comprising forming a doped well of a first conductivity type in [[the]]a substrate below a gate of the second transistor ~~gate~~.

58. (Currently amended) The method of claim 48, further comprising forming at least one doped well of a first conductivity type in [[the]]a substrate, wherein the first and second pinned photodiodes are formed within the substrate.

59. (Currently amended) The method of claim 58, wherein the act of forming the second ~~photo-conversion device~~ pinned photodiode comprises forming the second ~~photo-conversion device~~ pinned photodiode in the doped well.

60. (Currently amended) The method of claim 58, wherein the act of forming the first ~~photo-conversion device~~ pinned photodiode comprises forming the first ~~photo-conversion device~~ pinned photodiode outside of the doped well.

61. (Currently amended) The method of claim 58, wherein the act of forming the second ~~photo-conversion device~~ pinned photodiode comprises forming the second ~~photo-conversion device~~ pinned photodiode outside of the doped well.

62. (Currently amended) The method of claim 58, wherein the act of forming the at least one doped well comprises forming a doped well between the first and second ~~photo-conversion devices~~ pinned photodiodes.

63. (Currently amended) The method of claim 48, further comprising forming a ~~gate of a~~ second transistor, the act of forming the second transistor ~~gate~~ comprising forming [[the]]a gate of an output source follower transistor electrically connected to the second ~~photo-conversion device~~ pinned photodiode.

Claims 64-72 (Canceled).